Design of Low Phase Noise Ring VCO in 45NM Technology

Pankaj A. Manekar , Prof. Rajesh H. Talwekar

Abstract: -"CMOS" refers to both particular style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits. CMOS circuitry in VLSI dissipates less power when static, and is denser than other implementations having same functionality.[1]. This paper presents a framework for modeling the phase noise in complementary metal–oxide–semiconductor (CMOS) ring oscillators and is brief study of high performance VCO on 45 nm technology to achieve the desired objectives such as both non linear and linear operations. Maximum frequency limitations and associated noise performance levels of Ringoscillator are explored. The circuit used is a modified design of high performance VCO. In the estimated design more emphasis is given on power consumption, layout design and many more.

Index Terms—complementary metal–oxide–semiconductor (CMOS) ring oscillator, phase noise, timing jitter, voltage-controlled oscillator (VCO).

1 INTRODUCTION

Phase-locked loops (PLLs) are used extensively in communications systems. In Particular, they are used as frequency synthesizers and clock recovery circuits. Voltage-controlled oscillators (VCOs) are important building blocks in PLLs. The random fluctuations in the output phase of the oscillator, in terms of jitter or phase noise, are undesirable in most applications. The VCO is the major contributor to the PLL output phase noise outside the PLL loop bandwidth [1]. Hence VCOs with low phase noise have to be designed to meet latest communications standards. But, real oscillators are nonlinear time-variant systems such that traditional linear time-invariant analysis becomes invalid for phase noise studies [1]. The design of complementary metal–oxide–semiconductor (CMOS) VCOs with low phase noise is a challenging research topic and has been studied extensively in recent years. Many traditional oscillators are based on LC resonators. Due to the difficulties in the implementation of on-chip inductors and the limited frequency tuning range, resonatorless VCOs have drawn significant attention for system-on-a-chip solutions [4]. Among many possible circuit topologies, ring oscillators are promising candidates due to their ease of implementation and wide frequency tuning range.

They are compatible with digital CMOS technologies and occupy small chip area. However, because they do not have high- frequency selective elements, the phase noise for ring oscillators have traditionally been much larger than that of resonator-based oscillators. A new MOS model, called BSIM4, has been introduced in 2000.

A simplified version of this model is supported by Microwind 3.1, and recommended for ultra-deep submicron technology simulation. The role of oscillators is to create a periodic logic or analog signal with a stable and predictable frequency. Oscillators are required to generate the carrying signals for radio frequency transmission, but also for the main clocks of processors. The output is equal to the input, and the phase difference is equal to one fourth of the period ($\pi/2$) according to the phase Detector principles.

2 DESIGN METHODOLOGY

In the design, a simple Three stage Ring oscillator is explained with its structure and working methodology using CMOS technology and the disadvantages of this design structures are eliminated in advance circuitry.

- *Pankaj A.Manekar currently pursuing M.Tech Degree in Electronics and Telecommunication (VLSI & EMBEDDES SYSTEMS) from DIMAT,Raipur. (C.G.)*
- *E-mail: pankajmanekar.com*
  Prof. R.H Talwekar, HOD Electronics & Telecommunication Dept. , DIMAT, Raipur. (C.G.)

2.1 Basic Three Stage Ring VCO

The basic complemented metal semiconductor cell which is used to design all the circuits is shown in the fig.1 given below, which consists of PMOS and NMOS in complemented structure.

The ring oscillator is a very simple oscillator circuit, based on the switching delay existing between the input and output of an inverter. If we connect an odd chain of inverters, we obtain a natural oscillation, with a period which corresponds roughly to the number of elementary delays per gate [7]. The fastest oscillation is obtained with 3 inverters (One single inverter connected to itself does not oscillate). The usual implementation consists in a series of five up to one hundred chained inverters. Usually, one inverter in the chain is replaced by a NAND gate to enable the oscillation.

Fig. 2 shows a simplified model for a three-stage ring oscillator. Each delay stage consists of a resistor, a capacitor, a negative cell, and a voltage limiter. The system is linear as long as the internal voltages are not clipped by the limiters. When the peak-to-peak voltage swing exceeds the supply voltage of the circuit, the waveform becomes clipped by and ground, and this is modeled by the limiters in Fig.

2.2 Problems of Dai and Harjaani's three stage Ring oscillator model:-

The waveform is clipped when peak to peak voltage swing becomes greater than supply voltage provided to the circuit. Hence sinusoidal waveform is clipped by the circuit. The limiters are emplo7yed to model the clipping but their interference is effective for the improvement achieved upto soft clipping of the waveform which can be obtained.

.

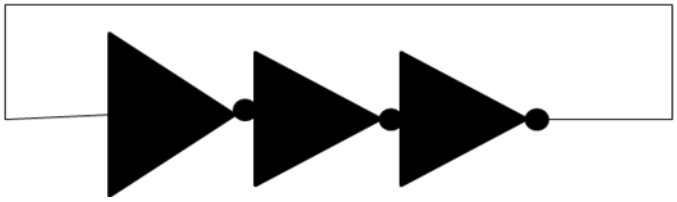

fig.1 (a) Basic Three Stage Ring VCO

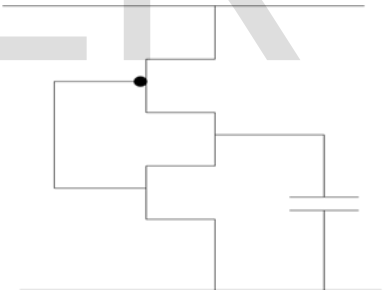

fig.1 (b) Basic CMOS cell

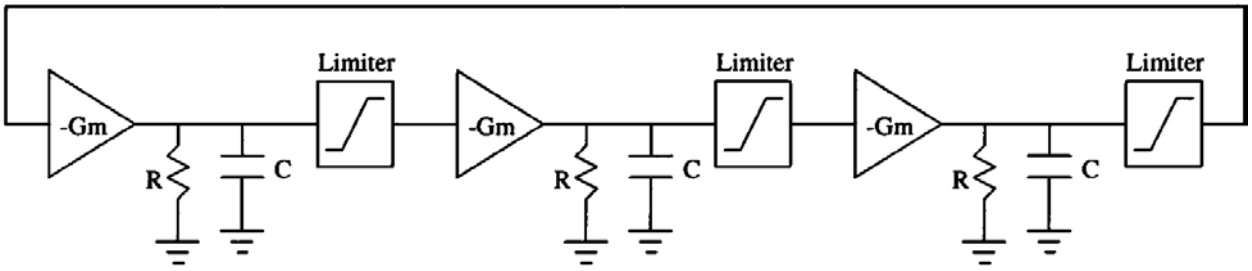

fig.2 DAI AND HARJANI: DESIGN OF LOW-PHASE-NOISE CMOS RING OSCILLATORS

3 Five stage High performance Ring Oscillator Model

If we connect an odd chain of inverters, we obtain a natural oscillation, with a period which corresponds roughly to number of elementary delays per gate[11].

The layout of 5 stage ring oscillator is shown in fig.3 below. The five stage ring oscillator model is simulated in Microwind 3.1 and implemented for the simulation in several test chips with successful results in different micrometer ranges. The implementation of the current starved for a five inverter chain using, 45nm VLSI technology is shown in following fig 3. Technology used is CMOS 45 nm, High/k/metal/strain-8 metal copper (1.00, 1.8v). In the layout the current mirror is situated in the left. Five inverters have been used to design the basic ring oscillator. The buffer inverter is kept on the right side of the layout, through which output Vhigh is measured.

4 Experimental Results & Discussion:

The simulation of a high performance Five stage Ring VCO circuit was carried out and is shown in fig. 4. In this simulation study, the performance of VCO circuit such as, frequency and voltage stability were revealed. It was verified that, the frequency remains constant at 5 GHz for the variation of voltage from 0.8 v to 1.6v in the steps of 0.2 v, hence the frequency stability is achieved and is clearly seen in fig.4

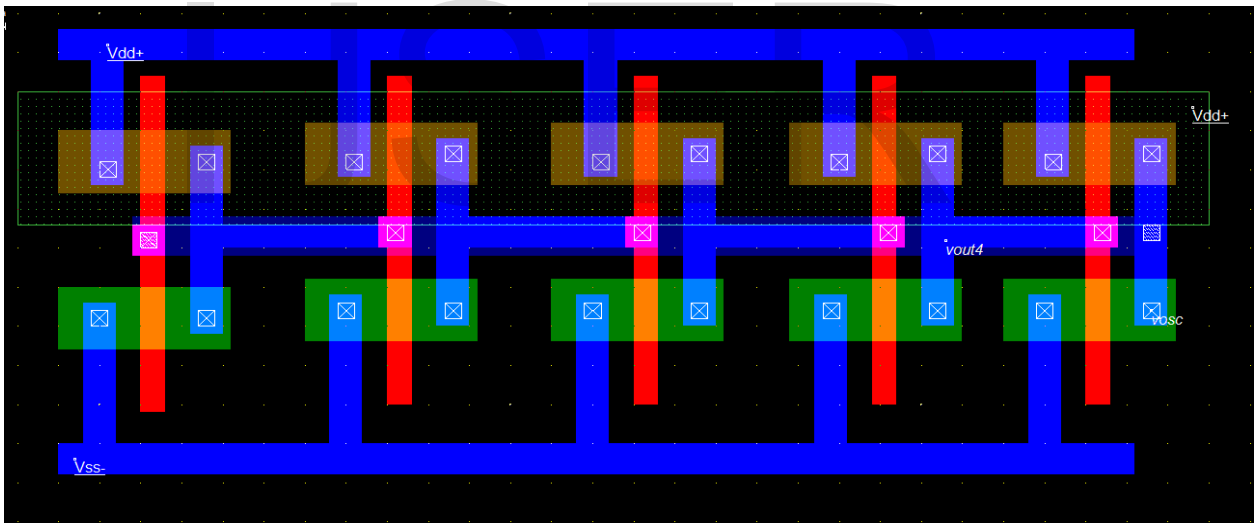

fig.3 Five stage Ring Oscillator Layout using Microwind 3.1

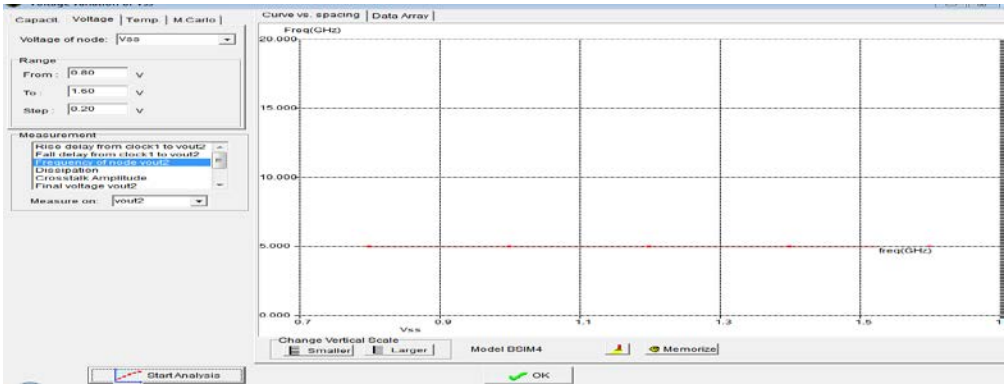

fig.4 Frequency analysis for 5 stage RING VCO

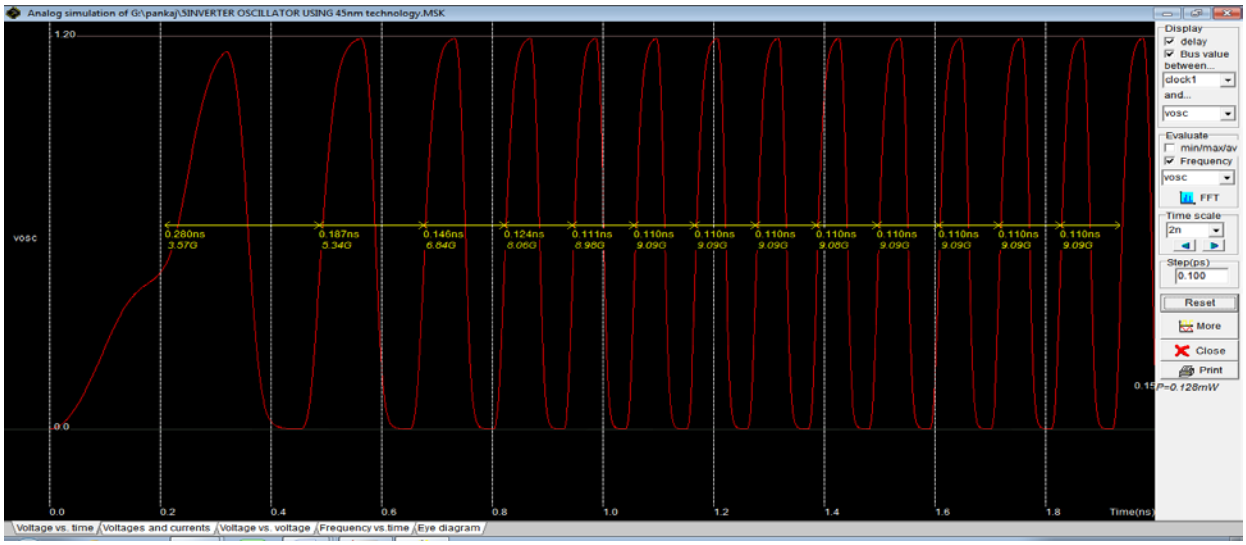

fig.5 Voltage Vs Time analysis

The dependence of oscillating frequency over the input voltage control is minimized and better stability is obtained. The voltage Vs Time analysis is shown in Fig. 5which shows the stable output obtained from five stage Ring oscillator.

The main drawback of this type of oscillator is the great influence of temperature and VDD supply on the stability of the oscillations. If the temperature changes, the device current changes, and consequently the oscillation frequency gets modified. Such oscillators are rarely used for high stability frequency generators. Another drawback of this Oscillator is Frequency of oscillation is not variable according to the requirement. Hence directly cannot be used in PLL circuit.

5 Conclusion

The physical layout design level of the circuit is possible in software used for integration and simulation of the model. The layout of VCO designed provides very high stability with respect to the input Voltage and remains stable for the variation upto level of 1.6 volt. In the estimated design of VCO, maximum focus is given on power consumption, layout design and related parameters. A brief study of high performance five stage Ring VCO on 45 nanometer VLSI technology is presented, where a reasonably good frequency stability and voltage stability was obtained experimentally through simulation.

References

[1] Liang Dai, *Member, IEEE,* and Ramesh Harjani, "Design of Low-Phase-Noise CMOS Ring Oscillators" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING, VOL. 49, NO. 5, MAY 2002

[2] Fernando Rangel De Sousa, "A reconfigurable high frequency phase-locked loop" *IEEE transaction actions on instrumentation & measurement* Vol. 53 No. 4 Aug. 2004.

[3] H. I. Cong et al., "Multigigahertz CMOS dual-modulus prescaler IC," *IEEE J. Solid-State Circuits,* vol. 23.

[4] www.microwind .com

[5] E. Sicard, S. Delman- Bendhia, "Advanced CMOS Cell Design", *Tata McGraw Hill* .

[6] E. Sicard, Syed MahfuzulAziz, "Introducing 45 nm technology in Microwind3*," Microwind application note*.

[7] M. Banu, "MOS oscillators with multi-decade tuning range and gigahertz maximum speed", *IEEE J.Solid-State Circuits*,vol. 23.

[8] N. Foroudi, "CMOS high-speed dual-modulus frequency divider for RF frequency synthesizers", *M. Eng. thesis*, Carleton University, Ottawa, Canada, 1991

[9] R. Rogenmoser et al., "1.16 GHz dual-modulus 1.2 _m CMOS prescaler", *IEEE Custom* IC's Conf., 1993.

[10] Gorth Nash, "Phase locked loop design fundamentals", *AN535* application note.

[11] Ms. Ujwala A. Belorkar 1 and Dr. S.A.Ladhake2 International Journal of Computer Networks & Communications (IJCNC), Vol.2, No.4, July 2010